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OF

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FOR

SEMICONDUCTOR ALLOY WITH LOW SURFACE ROUGHNESS, AND METHOD OF MAKING THE SAME

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BACKGROUND OF THE INVENTION

Field of the Invention

[0073] This invention relates to low surface roughness semiconductor alloys, more specifically to a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ material having low surface roughness, to heterostructures including such compositionally-graded material, e.g., $Si_{1-x}Ge_x$/Si material having low surface roughness, and to a process for producing such low surface roughness material and heterostructures including same.

Description of the Prior Art

[0074] In the production of epitaxial layers for fabrication of microelectronic devices, it has been demonstrated that forming epitaxial silicon layers under tensile strain can improve device performance. For example, Currie et al. in J. Vac. Sci. Technol. B 19(6), Nov/Dec 2001 describe performance enhancements of strained silicon devices over bulk silicon devices.

[0075] One technique for forming silicon under tensile strain involves depositing silicon onto a strain-relaxed $Si_{1x}Ge_x$ layer. Such strain-relaxed $Si_{1-x}Ge_x$ layer is sometimes referred to as a virtual substrate. Deposition of strained silicon layers onto virtual substrates has been an active area of research for a number of years (Fitzgerald et al, Appl. Phys. Lett., **59**, (1991) 811). The challenge in such virtual substrate processes is depositing a fully-relaxed, low defect, smooth $Si_{1-x}Ge_x$ layer to serve as an optimum substrate for the strained silicon deposition step and the subsequent device structure. Defects present in the virtual substrate (Larsen, Mat. Sci. and Eng. B71, (2000) 6-13) can propagate into the strained silicon layer and degrade device performance. A primary goal of the device builder using strain relaxed $Si_{1-x}Ge_x$ is to reduce the number of defects in the $Si_{1-x}Ge_x$ layer that can affect the strained Si layer.

[0076] A common approach to depositing strain-relaxed $Si_{1-x}Ge_x$ layers is compositionally grading the $Si_{1-x}Ge_x$ layer, so that it compositionally ranges over its thickness from pure silicon at one face of the material to the desired germanium concentration at the other face. Brasen et al. U.S. Patent Number 5,221,413 discloses a method of forming compositionally-graded $Si_{1-x}Ge_x$ layers at temperatures in excess of 850°C.

Legoues et al. U.S. Patent Number 5,810,924 also describes a process of forming compositionally-graded $Si_{1-x}Ge_x$ layers. In the approach described in these references, a reduction of misfit and threading dislocations is attributed to the compositional grading process. Compositional grading reduces the driving force for misfit dislocation and associated threading dislocation formation through a continuum of low mismatch interfaces in the graded region. Threading dislocations, which intersect the surface of the film, have the potential to move across a wafer and be annihilated at the edge of the wafer during this process.

[0077] Compositional grading of $Si_{1-x}Ge_x$ has resulted in threading dislocation density levels as low as $10^5/cm^2$, as reported by Leitz et al, J. Appl. Phys., Vol. 90, No. 6, 15 September 2001. Misfit dislocations, however, typically remain at the interface where they have formed, each creating a small displacement in the vertical direction in the crystal lattice. The vertical displacements can combine to create larger vertical displacements and localized strain in the film, with a resulting three-dimensional roughening of the surface commonly referred to as cross-hatch. Severe cross-hatch will render the surface of the film unsuitable for device formation, since subsequent strained silicon layers deposited on the excessively roughened $Si_{1-x}Ge_x$ surface will have degraded device performance.

[0078] While the cross-hatch surface roughness in compositionally-graded $Si_{1-x}Ge_x$ layers has been correlated with the occurrence of misfit dislocations, the exact mechanism affecting the degree of the cross-hatch phenomenon has been the subject of continuing study. Hsu et al. (Appl. Phys. Lett., **61**, (1992) 1293) has reported that strain fields associated with the misfit dislocation influence the local growth rate, increasing the roughness of the cross-hatch. This finding has been confirmed by Yu et al. (Appl. Phys. Lett., Vol.64, No. 24, 13 June 1994, 3305). Li et al. (J. Vac. Sci. Technol. B 16(3), May/June 1998), however, reported that surface roughness is a primarily a result of a summation of misfit slip steps due to the dislocations, while acknowledging that three-dimensional growth may be affected by periodic variations in the surface.

[0079] Process conditions that have been reported to modify the degree of cross-hatch have primarily involved the grading rate of the $Si_{1-x}Ge_x$ layer and deposition temperature. For a $Si_{1-x}Ge_x$, x=0.2 final concentration, the aforementioned Li et al. reference reported that low grading rates of 5%Ge/μm were

necessary to achieve a surface roughness of 1.4 nm. Pidduck et al. (Proceedings Microsc. Semicond. Mater. Conf., Oxford, 7-10 April 1997) reported a surface roughness of 2-6 nm for $Si_{1-x}Ge_x$, x=0.23 at a grading rate of 5% Ge/μm. Pidduck also reported that higher temperatures, of $\geq$ 800°C, are necessary. Kazuki et al. (Mat. Res. Soc. Symp. Proc. Vol. 648, 2001) reported surface roughness results for $Si_{1-x}Ge_x$, x=0.3 for three grading schemes (linear grading, step and step-graded) at temperatures of 650-800°C at 5-30% Ge/μm, in which the best roughness values were 1.2 nm at 5% Ge/μm.

[0080] The foregoing studies reflect the fact that the best surface roughness heretofore achieved by the art in fully-relaxed, compositionally-graded $Si_{1-x}Ge_x$, $x \leq 0.3$ layers is in excess of 1.0 nm.

[0081] The efforts to minimize surface roughness is complicated by the fact that such efforts have concurrently produced undesirably high levels of threading dislocation density. For example, in reducing the surface roughness from 3 nm to 1.2 nm through appropriate selection of growth conditions, threading dislocation density may increase from $4x10^4/cm^2$ to $4x10^5/cm^2$.

[0082] To date, no process has been reported that enables surface roughness $\leq$ 1.0 nm to be obtained in a fully-relaxed, compositionally-graded $Si_{1-x}Ge_x$, $x \leq 0.3$ material, while achieving a threading dislocation density $< 1 \times 10^5$ threading dislocation defects/cm^2 of surface area.

SUMMARY OF THE INVENTION

[0083] The present invention relates to low surface roughness semiconductor alloys, more specifically to a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ material having low surface roughness, wherein $0 < x < 1$, as well as to heterostructures including such compositionally-graded material, e.g., $Si_{1-x}Ge_x$/Si material having low surface roughness, and to a process for producing such low surface roughness material, and heterostructures including same.

[0084] In one aspect, the invention relates to a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ material having a surface roughness of less than 1 nm, wherein $0 < x < 1$.

[0085] In another embodiment, the invention relates to a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ ($x \leq 0.3$) material with surface roughness less than 1 nm, and threading dislocation density < 1 x 10^5 threading dislocation defects/cm^2 of surface area.

[0086] A further aspect of the invention relates to an epitaxial heterostructure, comprising a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ epitaxial layer having a surface roughness of less than 1 nm, wherein $0 < x < 1$, and a heterostructural material deposited on the compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ epitaxial layer.

[0087] A still further aspect of the invention relates to a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ epitaxial layer on a substrate formed by a process comprising contacting silicon and germanium precursor gases with the substrate under vapor deposition conditions comprising controlled temperature ramping, wherein the compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ epitaxial layer has a surface roughness of less than 1 nm and a threading dislocation density less than 1 x 10^5 threading dislocation defects/cm^2 of surface area.

[0088] In another aspect, the invention relates to a method of forming on a substrate a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ ($0 < x < 1$) epitaxial layer having a surface roughness of less than 1 nm, the method including contacting silicon and germanium precursors with the substrate under $Si_{1-x}Ge_x$ ($0 < x < 1$) epitaxial layer growth conditions, and varying temperature, e.g., by ramping of temperature, during at least part of such contacting.

[0089] As used in such context, the term "ramping" in reference to temperature means that the temperature in the silicon and germanium precursors contacting step is continuously varied, e.g., in a linear or non-linear fashion, during at least part of the contacting step.

[0090] As used herein, the term "surface roughness" means average surface roughness as measured by atomic force microscope (AFM) on a 10μm x 10μm area of the surface of the graded $Si_{1-x}Ge_x$ ($0 < x < 1$) material.

[0091] Other aspects, features and embodiments of the invention will be more fully apparent from the ensuing disclosure and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 is a graph of germanium concentration in atomic percent as a function of thickness in a graded 2μm thick $Si_{1-x}Ge_x$ layer (line A), with lines B and C showing deposition temperature, in °C, as a function of layer thickness during the deposition process.

[0021] FIG. 2 is a graph of deposition temperature, in °C, as a function of germanium concentration, in atomic percent, of a $Si_{1-x}Ge_x$ layer formed in accordance with the present invention.

[0022] FIG. 3 is an Arrhenius plot of $Si_{1-x}Ge_x$ deposition rate, in Å/minute, as a function of the inverse deposition temperature, in units of 10^3 $°K^{-1}$, for a $Si_{1-x}Ge_x$ layer formed in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION, AND PREFERRED EMBODIMENTS THEREOF

[0023] The present invention relates to a compositionally-graded, strain-relaxed $Si_{1-x}Ge_x/Si$ material having average surface roughness of less than 1 nanometer (nm), and to a process for producing such low surface roughness material.

[0024] The compositionally-graded $Si_{1-x}Ge_x$ layer of the invention provides a suitable base for growth of strained silicon or heterostructure materials such as SiGe, Si, Ge, GaAs, etc., at average surface roughness below 1 nm.

[0025] While the compositionally-graded $Si_{1-x}Ge_x$ layer of the invention can be formed in any suitable manner, a preferred approach utilizes a chemical vapor deposition operation (e.g. reduced pressure chemical vapor deposition, high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition or the like) for contacting silicon and germanium precursor gases with the substrate to form the compositionally-graded $Si_{1-x}Ge_x$ layer. The $Si_{1-x}Ge_x$ layer is grown with a gradual increase in Ge-content from pure silicon at the interface with the silicon substrate, to some ultimate composition (Ge

concentration) at the top surface of the $Si_{1-x}Ge_x$ layer. A final capping layer may then be grown at the ultimate composition, followed by strained silicon or some combination of heterostructure material.

[0026] We have discovered that during the chemical vapor deposition of a compositionally-graded $Si_{1-x}Ge_x$ layer, the amount of surface roughness varies with the growth temperature, and therefore that temperature can be modulated during the growth process to produce a compositionally-graded $Si_{1-x}Ge_x$ layer having extremely low roughness, below levels that have heretofore been obtainable in the art. The surface roughness of compositionally-graded $Si_{1-x}Ge_x$ films in the practice of the present invention is < 1 nm, and more preferably ≤ 0.9.

[0027] The effect of growth temperature on the surface roughness of the compositionally-graded $Si_{1-x}Ge_x$ layer is shown by the data in Table 1 below. This table sets out the average surface roughness, in nm, for a 10μm x 10μm surface area, as determined by atomic force microscope (AFM), for a series of compositionally-graded $Si_{1-x}Ge_x$ layers, grown at different growth temperatures (800°C, 850°C and 900°C), $Si_{1-x}Ge_x$ graded layer thickness, in μm, and capping layer $Si_{0.8}Ge_{0.2}$ thickness, in μm.

[0028] Table 1 - Surface roughness for $Si_{0.8}Ge_{0.2}$ layers on graded (10%Ge/μm) $Si_{1-x}Ge_x$

Growth Temperature, °C	$Si_{1-x}Ge_x$ Grade Thickness, μm	Thickness of Capping $Si_{0.8}Ge_{0.2}$, μm	Average Roughness, nm 10μm x 10μm, AFM
900	2.0	2.0	2.5
850	1.5	1.5	2.0
800	2.0	2.0	0.9

[0029] The data in Table 1 show that for $Si_{0.8}Ge_{0.2}$ layers deposited onto a compositionally-graded layer, the surface roughness is a function of the growth temperature, with lower growth temperatures producing smoother films. The smoothest film had an average surface roughness of 0.9 nm at a growth temperature of 800°C.

[0030] Unfortunately, films grown at lower temperatures have higher levels of threading dislocation densities than corresponding films grown at higher temperatures. Accordingly, the requirements of concurrently obtaining smooth films for semiconductor device manufacture, and low levels of threading

dislocation defects, are opposed to one another in respect of the growth temperature regimes that may be employed.

[0031] The approach of the present invention, rather than attempting to synthesize these competing requirements in favor of a single growth temperature that will yield low surface roughness and low levels of threading defects, is to modulate the growth temperature during the growth of the graded $Si_{1-x}Ge_x$ layer, to achieve a strikingly lower level of threading defects and surface roughness than is possible with isothermal growth processes.

[0032] Table 2 illustrates the unexpected improvement that results from modulation of temperature conditions during the growth of the graded $Si_{1-x}Ge_x$ layer. Data are shown for three different growth temperature regimes, one in which isothermal growth is conducted at a temperature of 800°C, another in which isothermal growth is conducted at a temperature of 900°C, and a third in which temperature ramping was carried out as hereinafter more fully described.

[0033] Table 2 - Surface roughness and threading dislocation density

Growth Temperature, °C	**Threading Dislocation Density, cm^2**	**Average Roughness, nm 10μm x 10μm, AFM**
800	4×10^5	0.9
900	4×10^4	2.5
Temperature Ramp	4×10^4	0.9

[0034] Table 2 shows the impact of growth temperature on both threading dislocation density and roughness. Although an isothermal growth of the $Si_{1-x}Ge_x$ layer at 800°C produced an average AFM surface roughness of 0.9 nm, the threading defect density was high at 4×10^5 threading defects/cm^2. By increasing the temperature of the isothermal growth regime to 900°C, the threading defect density was decreased to 4×10^4 threading defects/cm^2, but the average surface roughness increased dramatically, to 2.5 nm. In contrast to these isothermal approaches, the temperature ramping approach of the present invention produced a graded $Si_{1-x}Ge_x$ material that exhibited a 10-fold reduction in threading defects from the level achieved at

800°C, with a surface roughness that was over 60% lower than the level achieved by isothermal growth at 900°C.

[0035] Thus, the ramped temperature growth technique of the present invention produced a graded $Si_{1-x}Ge_x$ film having a combination of low surface roughness (< 1 nm) and low dislocation defect density (< 1 x 10^5 threading defects/cm^2, preferably < 5 x 10^4 threading defects/cm^2) that were unachievable by either isothermal technique alone.

[0036] The ramped growth process producing the data shown in Table 2 included ramping of temperature as well as ramping of germane (GeH_4) flow rate. The ramped growth process was conducted at a pressure of 20 Torr, a flow rate of 25 standard liters per minute of hydrogen gas (H_2), and a flow rate of 100 standard cubic centimeters per minute (sccm) of dichlorosilane (DCS).

[0037] The process included two phases, with the first phase involving ramping of germane flow rate at a constant temperature of 900°C, and with germane flow rate being progressively increased during the successive time periods of the process, as set out in Table 3.

[0038] The second phase of the process involved ramping of temperature at a constant flow rate of germane of 60 standard cubic centimeters per minute (sccm), with the temperature being progressively decreased over successive 30 second intervals as set out in Table 4.

[0039] In both phases the flow rate of germane is set out for a stream containing 10% by weight GeH_4 in hydrogen carrier gas.

[0040] Table 3

GeH_4 flow ramping @ 900°C
(Process Conditions: 20 Torr, 25 slm H_2, 100 sccm DCS)

GeH_4(10%), sccm	Deposition time, sec
0-18	155
18-31	110
31-44	97
44-60	105

[0041] Table 4

Temperature Ramping @ 60 sccm GeH_4 (10%)
(Process Conditions: 20 Torr, 25 slm H_2, 100 sccm DCS)

Deposition temperature, °C	Deposition time, sec
900-883	30
883-872	30
872-861	30
861-850	30
850-842	30
842-834	30
834-826	30
826-817	30
817-809	30
809-803	30
803-796	30
796-790	30
790-784	30
784-778	30

[0042] After forming the graded $Si_{1-x}Ge_x$ film by the ramped technique described above, the film was capped with a constant-composition layer of $Si_{0.8}Ge_{0.2}$ for analysis.

[0043] In the illustrative embodiment of the ramped graded $Si_{1-x}Ge_x$ film forming process of the invention, the process was begun at 900°C to avoid significant spontaneous gas-phase nucleation and excessive coating of the gas-phase reactor chamber in which the deposition was carried out, such as were observed when carrying out the process at higher temperatures. It will nonetheless be recognized that specific temperature conditions will vary in the broad practice of the invention, with respect to the specific matrix of process conditions employed, the gas-phase reactor utilized, and the specific precursors that are employed, as can be readily determined without undue experimentation, based on the disclosure hereof.

[0044] Further, while vapor deposition techniques are preferred for forming the graded $Si_{1-x}Ge_x$ film in the practice of the invention, it will be recognized that other film-forming techniques can advantageously be employed, and will require corresponding variation of process conditions based on similar considerations, as is readily determinable within the skill of the art, based on the disclosure herein.

[0045] Preferred growth temperature ranges usefully employed in the practice of the ramped temperature process of the present invention will depend on the ultimate composition of the SiGe "virtual substrate" that is produced by the inventive process. In general, however, it is preferred to begin the compositional grading growth process at temperature on the order of approximately 900°C or higher depending on the specific precursor (source reagent) chemistry that is employed. For an ultimate (grown material top surface) composition of $Si_{0.8}Ge_{0.2}$, it is preferred that the final stages of the growth process are carried out at temperature on the order of approximately 800°C, e.g., in a range of from about 775°C to about 825°C). Similar results can be achieved for higher ultimate Ge-content at final growth temperatures below 800°C.

[0046] The temperature ramping process of the invention is to be distinguished from the Molecular Beam Epitaxy (MBE) technique disclosed in Brasen et al. U.S. Patent 5,221,413. In MBE reactors, it is necessary to grow under conditions that maintain a low vapor pressure, since germanium otherwise will tend to evaporate. Brasen fails to describe a suitable method for producing as-grown films with roughness levels below 1 nm. Although Brasen describes growing CVD films at ~900°C, we have found that surface roughness tends to degrade at this temperature once the peak Ge-content of the film exceeds about 10 atomic percent Ge. The temperature ramping technique of the present invention overcomes such deficiency and permits superior results to be achieved at Ge-content levels above 10 atomic percent.

[0047] Similar distinction is applicable to the process described in Bensahel et al. U.S. Patent 6,117,750, which utilizes low temperatures and is unable to achieve the superior surface smoothness that is characteristic of the graded $Si_{1-x}Ge_x$ films produced by the method of the present invention.

[0048] The temperature ramping in the practice of the invention can be carried out in a linear or non-linear manner, as regards the progressive change of the growth temperature. The temperature ramping can be conducted concurrently with ramping of the germanium source, e.g., germane, so that temperature and Ge source material flow rate are each contemporaneously varied in the course of the growth operation. The ramping procedure may be carried out during the entire growth process, or alternatively, ramping may be carried out only during a portion of the growth process, as necessary or desirable in a given application of the invention.

[0049] The process of the invention may be employed to form step or step-graded $Si_{1-x}Ge_x$ films.

[0050] Any suitable deposition techniques may be employed to form the low defect density, low surface roughness $Si_{1-x}Ge_x$ films of the invention, with chemical vapor deposition techniques being most preferred. CVD may be carried out at any suitable conditions within the scope of the disclosure herein, including techniques such as reduced pressure CVD, ultra-high vacuum CVD, atmospheric pressure CVD, plasma-assisted CVD, etc.

[0051] Germanium and silicon source materials useful in forming the low defect density, low surface roughness $Si_{1-x}Ge_x$ films of the invention may be of any suitable type, including germanium sources such as germane (GeH_4), halogermanes whose halo moiety is chlorine, fluorine, iodine or bromine, such as chlorogermanes of the formula GeH_xCl_{4-x} wherein x is an integer having a value of from 1 to 3 inclusive, and silicon sources such as silane (SiH_4), Si_3H_8, Si_2H_6 and halosilanes whose halo moiety is chlorine, fluorine, iodine or bromine, such as chlorosilanes of the formula SiH_xCl_{4-x} wherein x is an integer having a value of from 1 to 3 inclusive.

[0052] After the low defect density, low surface roughness $Si_{1-x}Ge_x$ material of the invention is formed, a capping layer may then be grown. The capping material may be $Si_{1-x}Ge_x$ grown at the ultimate composition of the underlying top surface $Si_{1-x}Ge_x$ material, followed by strained silicon or other heterostructural material (e.g., Ge, GaAs, AlAs, AlGaAs, etc., and related ternary and quaternary semiconductors), or strained silicon or other heterostructural material may simply be formed on the low defect density, low surface roughness $Si_{1-x}Ge_x$ material without an intervening $Si_{1-x}Ge_x$ capping layer, as necessary or desired in a given application of the present invention.

[0053] The $Si_{1-x}Ge_x$ material of the invention may be formed at any suitable film thickness necessary or desirable in a given application of the invention. In one embodiment, the $Si_{1-x}Ge_x$ material is formed in a thin film having a material thickness of 0.01 μm to 3,000 μm, although greater or lesser film thicknesses may be employed in the broad practice of the invention, depending on the specific application of the graded silicon-germanium layer.

[0054] Referring now to the drawings, FIG. 1 is a graph of germanium concentration in atomic percent as a function of thickness in a graded 2μm thick $Si_{1-x}Ge_x$ layer (line A), with lines B and C showing deposition temperature, in °C, as a function of layer thickness during the deposition process.

[0055] Curve A in Fig. 1 shows a linear grade in germanium in a $Si_{1-x}Ge_x$ layer, corresponding to a compositional grading rate of 10% Ge/μm. Curve C describes the temperature ramp conditions used in the illustrative embodiment described hereinabove in connection with Tables 3 and 4 hereof, and Curve B is an alternative temperature ramp for achievement of comparable results. Curve B describes the simplest case of a linear temperature ramp over the entire range of film thickness. In the process corresponding to curve C, an initial portion of the $Si_{1-x}Ge_x$ layer is grown at constant temperature followed by growth of the remainder of the $Si_{1-x}Ge_x$ layer under temperature ramping conditions. During the constant temperature portion of the process, the flow rate of the germanium source, GeH_4, is varied to control the linear grading of the germanium concentration in the film. Temperature ramping, as indicated hereinabove, may be linear or non-linear as regards the change of temperature during the relevant portion of the growth process in which the temperature is varied.

[0056] To determine the conditions necessary for the temperature ramping profile shown in FIG. 1, the process data shown in FIGS. 2 and 3 was collected.

[0057] FIG. 2 is a graph of deposition temperature, in °C, as a function of germanium concentration, in atomic percent, of a $Si_{1-x}Ge_x$ layer formed in accordance with the present invention.

[0058] FIG. 3 is an Arrhenius plot of $Si_{1-x}Ge_x$ deposition rate, in Å/minute, as a function of the inverse deposition temperature, in units of $10^3 \times {}^\circ K^{-1}$, for a $Si_{1-x}Ge_x$ layer formed in accordance with the present invention.

[0059] In generating the graph of FIG. 2, the germanium concentration in an epitaxial layer was recorded for a specific set of process conditions while the deposition temperature was varied. The variable temperature was recorded on the y-axis to facilitate use of the data in establishing the temperature ramp. FIG. 3 is an Arrhenius plot of deposition rate versus temperature from the same set of experiments used to generate FIG. 2. To construct the temperature ramp, the endpoint germanium concentrations in the $Si_{1-x}Ge_x$

graded film were first specified. For the curve in FIG. 2, the lowest germanium concentration indicated was 15% at 900°C. This was the lower starting concentration for the set of conditions under which these data were collected. Similar to curve C in FIG. 1, the beginning of the temperature ramp in this case was at 15% germanium concentration. Lower initial concentrations are possible by simply adjusting the process conditions and constructing a curve similar to the one in FIG. 2. In the case where the $Si_{1-x}Ge_x$ layer was to be graded to 25% germanium concentration, the final temperature was determined to be approximately 780°C. Thus, the temperature was determined to be linearly graded from 900°C to 780°C.

[0060] The FIG. 3 Arrhenius plot was used to calculate the deposition time at each temperature interval in the temperature ramp, to obtain the compositional grading in curve A of FIG. 1.

[0061] In another illustrative embodiment, linear temperature ramping was carried out over the entire growth of the graded $Si_{1-x}Ge_x$ layer as set out in Table 5 below, at the process conditions set out in the header of such table for pressure (in Torr), hydrogen gas flow rate (in standard liters per minute), dichlorosilance flow rate (in standard cubic centimeters per minute) and germane flow rate (in standard cubic centimeters per minute, of a 10% by weight germane in hydrogen carrier gas).

[0062] Table 5

Deposition Time for Temperature Ramping
(Process Conditions: 10 Torr, 30 slm H_2, 100 sccm DCS, 20 sccm GeH_4(10%))

Deposition Temperature, °C	Deposition Time, min
900-840	20
840-800	20
800-770	20
770-745	20
745-735	20
735-720	20
720-700	25

[0063] At the beginning of the deposition process, the temperature was 900°C and was linearly ramped for 20 minutes to 840°C. The linear temperature ramping was continued in 20-minute segments until a temperature of 700°C was reached. The temperature ramp alternatively could have been segmented into

smaller or larger time intervals, as necessary or desirable to form the graded $Si_{1-x}Ge_x$ layer in a specific application of the present invention. The film was then capped with a constant-composition layer of $Si_{0.8}Ge_{0.2}$ for analysis.

[0064] It is possible to use temperature-ramped growth to increase the average grading rate of the $Si_{1-x}Ge_x$ film, while still maintaining acceptable defect levels and surface roughness. The advantages of increasing the grading rate include (i) reducing the processing time and cost of the $Si_{1-x}Ge_x$ film formation process, and (ii) forming thinner $Si_{1-x}Ge_x$ film layers of improved heat conduction characteristics, since SiGe alloys have lower thermal conductivity than pure silicon, and thinner films therefore improve heat conduction in electronic devices fabricated on such layers.

[0065] In another illustrative embodiment of the invention, a $Si_{1-x}Ge_x$ thin film was formed in which grading began at nominally 10 atomic % Ge per micron of film thickness, but at increased concentration of atomic % Ge, the grading rate was increased to 40 atomic % Ge per micron of film thickness, producing a $Si_{1-x}Ge_x$ thin film with a defect density of 1.1 x 10^5 threading dislocation defects/cm^2, and a surface roughness of 0.9 nm.

[0066] The data for the isothermal ramping of the germane flow rate in the initial portion of such process are set out in Table 6 below, together with the process conditions of pressure (in Torr), flow rate of hydrogen gas (in standard liters per minute), flow rate of dichlorosilane (in standard cubic centimeters per minute), and flow rate of hydrogen chloride (in standard cubic centimeters per minute).

[0067] Table 6

Initial portion of $Si_{1-x}Ge_x$ film-forming process - Isothermal ramping at 10%/micron thickness. (Process Conditions: 20 Torr, 20/5 slm H_2, 100 sccm DCS, 100 sccm HCl) Ramp began at 0% Ge and ended at 10% Ge.

GeH_4 Ramp @900°C	
GeH_4 (10%), sccm	Deposition time, sec
6	10
18	146
31	110

44	97
60	105

[0068] The data for the temperature ramping in the subsequent portion of the $Si_{1-x}Ge_x$ film-forming process are set out in Table 7 below, together with the process conditions of pressure (in Torr), flow rate of hydrogen gas (in standard liters per minute), flow rate of dichlorosilane (in standard cubic centimeters per minute), and flow rate of hydrogen chloride (in standard cubic centimeters per minute).

[0069] **Table 7**

Subsequent portion of $Si_{1-x}Ge_x$ film-forming process - Temperature Ramping at 40% Ge/micron thickness
(Process Conditions: 20 Torr, 20/5 slm H_2, 100 sccm DCS, 100 sccm HCl)
Ramp began at 10%Ge and ended at 20% Ge.

Temperature Ramp @ 60sccm GeH_4		
T, °C	**Temp Ramp, °C/sec**	**Deposition time, sec**
900-775	1	125

[0070] The $Si_{1-x}Ge_x$ film then was capped with a constant-composition layer of $Si_{0.8}Ge_{0.2}$ for analysis.

[0071] The foregoing illustrative embodiments reflect the advantages of the process of the present invention in forming graded $Si_{1-x}Ge_x$ ($0 < x < 1$) films that possess low surface roughness and low threading dislocation density, e.g., $< 1 \times 10^5$ threading dislocation defects/cm^2 of surface area. Such low surface roughness, low threading dislocation density compositionally-graded material is usefully employed for fabricating heterostructures such as $Si_{1-x}Ge_x$/Si structures.

[0072] The process of the invention as illustratively described herein is readily carried out in a simple manner, e.g., using chemical vapor deposition techniques, wherein temperature is selectively modulated during the growth of the graded $Si_{1-x}Ge_x$ ($0 < x < 1$) material, optionally with modulation of the precursor flow rate to the substrate, to produce virtual substrate structures amenable to coating with strained lattice material such as strained silicon. In a particularly preferred embodiment, the process of the invention is

conducted to produce compositionally-graded, strain-relaxed $Si_{1-x}Ge_x$ ($x \leq 0.3$) material with surface roughness less than 1 nm, and threading dislocation density < 1 x 10^5 threading dislocation defects/cm^2 of surface area.

[0073] It will therefore be appreciated that while the invention has been illustratively described herein with reference to particular aspects, features and embodiments, the invention may be practiced with variations and modifications and in other embodiments, as will suggest themselves to those of ordinary skill in the art, based on the disclosure herein. Accordingly, the invention is intended to be broadly interpreted and construed to encompass all such variations, modifications and other embodiments, as being within the spirit and scope of the claims hereinafter set forth.